WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device having memory cells each comprising:

a well of a first conductivity type formed in a semiconductor substrate;

a pair of semiconductor regions of a second conductivity type formed in said well of the first conductivity type, said pair of semiconductor regions being used as a source and a drain;

a first gate formed on the semiconductor substrate via a first gate insulator;

a second gate formed on a second insulator film covering said first gate; and

a third gate formed via the second insulator film relative to said first gate and via a third insulator film relative to said second gate,

wherein an impurity doped region of the first conductivity type having an impurity concentration higher than said well is formed in a channel region between said pair of semiconductor regions, said impurity doped region being not in contact with said semiconductor regions.

2. A nonvolatile semiconductor memory device according to claim 1, wherein the channel region is formed overlapping under two gates among said first to third gates, and the impurity doped region in the channel region is formed overlapping under the two gates.

3. A nonvolatile semiconductor memory device according to claim 1, wherein the impurity doped region is continuously formed along a channel width direction.

4. A nonvolatile semiconductor memory device according to claim 2, wherein the impurity doped region is continuously formed along a channel width direction.

5. A nonvolatile semiconductor memory device according to claim 1, wherein the impurity doped region extends in a depth direction of the semiconductor substrate deeper than said semiconductor regions.

6. A nonvolatile semiconductor memory device according to claim 2, wherein the impurity doped region extends in a depth direction of the semiconductor substrate deeper than said semiconductor regions.

7. A nonvolatile semiconductor memory device according to claim 3, wherein the impurity doped region extends in a depth direction of the semiconductor substrate deeper than said semiconductor regions.

8. A nonvolatile semiconductor memory device according to claim 4, wherein the impurity doped region extends in a depth direction of the semiconductor substrate deeper than said semiconductor regions.

9. A nonvolatile semiconductor memory device according to claim 1, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

10. A nonvolatile semiconductor memory device according to claim 1, wherein the first conductivity

type is an n-type and the second conductivity type is a p-type.

11. A nonvolatile semiconductor memory device according to claim 9, wherein p-type impurities are boron and n-type impurities are arsenic.

12. A nonvolatile semiconductor memory device according to claim 10, wherein n-type impurities are phosphorous and p-type impurities are boron.

13. A nonvolatile semiconductor memory device according to claim 1, wherein one of said first to third gates functions as an erase gate.

14. A nonvolatile semiconductor memory device according to claim 2, wherein one of said first to third gates functions as an erase gate.

15. A nonvolatile semiconductor memory device having memory cells each comprising:

a semiconductor substrate having at least a first conductivity type region on a principal surface of said semiconductor substrate;

a pair of semiconductor regions of a second conductivity type formed in the first conductivity type region, said pair of semiconductor regions being used as a source and a drain;

a first gate formed above a channel region between said semiconductor regions via a first insulator film; and

a second gate formed on said first gate via a second insulator film,

wherein in a partial area of the channel region, a heavily impurity doped region of the first conductivity type is formed having a higher impurity concentration than the first conductivity type region, and the heavily impurity doped region is spaced from any one of the semiconductor regions.

16. A nonvolatile semiconductor memory device according to claim 15, wherein the heavily doped impurity region is formed in the first conductivity type region under said first gate.

17. A nonvolatile semiconductor memory device according to claim 15, wherein the heavily impurity doped region is continuously formed along a channel width direction.

18. A nonvolatile semiconductor memory device according to claim 16, wherein the heavily impurity doped region is continuously formed along a channel width direction.

19. A nonvolatile semiconductor memory device according to claim 15, wherein the heavily impurity doped region is deeper than said semiconductor regions.

20. A nonvolatile semiconductor memory device according to claim 16, wherein the heavily impurity doped region is deeper than said semiconductor regions.

21. A nonvolatile semiconductor memory device according to claim 17, wherein the heavily impurity doped region is deeper than said semiconductor regions.

22. A nonvolatile semiconductor memory device

according to claim 18, wherein the heavily impurity doped region is deeper than said semiconductor regions.

23. A nonvolatile semiconductor memory device according to claim 15, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

24. A nonvolatile semiconductor memory device according to claim 15, wherein the first conductivity type is an n-type and the second conductivity type is a p-type.

25. A nonvolatile semiconductor memory device according to claim 23, wherein p-type impurities are boron and n-type impurities are arsenic.

26. A nonvolatile semiconductor memory device according to claim 24, wherein n-type impurities are phosphorous and p-type impurities are boron.

27. A nonvolatile semiconductor memory device according to claim 15, wherein said first gate is a floating gate and said second gate is a control gate.

28. A nonvolatile semiconductor memory device according to claim 16, wherein said first gate is a floating gate and said second gate is a control gate.

29. A manufacture method for a nonvolatile semiconductor memory device comprising:

a step of forming a well of a first conductivity type in a semiconductor substrate;

a step of forming a pair of semiconductor regions of a second conductivity type formed in the

well of the first conductivity type, the pair of semiconductor regions being used as a source and a drain;

a step of forming a first gate on the semiconductor substrate via a first gate insulator;

a step of forming a second gate on a second insulator film covering the first gate; and

a step of forming a third gate via the second insulator film relative to the first gate and via a third insulator film relative to the second gate,

wherein an impurity doped region of the first conductivity type having an impurity concentration higher than the well is formed in a channel region between the pair of semiconductor regions, the impurity doped region being not in contact with the semiconductor regions.

30. A manufacture method for a nonvolatile semiconductor memory device according to claim 29, wherein the semiconductor regions and the impurity region are formed in a self-alignment manner by tilted ion implantation tilted in opposite directions from a normal of the semiconductor substrate, by using one of the first to third gates as a mask.

31. A manufacture method for a nonvolatile semiconductor memory device according to claim 29, wherein the gate used as a mask for forming the impurity region through tilted ion implantation is one of a single layer film of polysilicon, a stacked film

of a polysilicon film and a silicon oxide film, a stacked film of a polysilicon film and a silicon nitride film, and a stacked film of a polysilicon film, a silicon oxide film and a silicon nitride film.

32. A manufacture method for a nonvolatile semiconductor memory device, comprising:

a step of forming dummy gates on a semiconductor substrate having a first conductive type region on a surface thereof;

a step of forming a pair of source/drain diffusion layers of a second conductivity type in a surface layer of the semiconductor substrate between adjacent dummy gates, by using the dummy gates as a mask;

a step of burying the dummy gates with a first insulator film;

a step of removing a portion of the first insulator film to expose an upper surface of each dummy gates without exposing the surface of the semiconductor substrate;

a step of removing the dummy gates;

a step of depositing a silicon nitride film or a polysilicon film on an upper surface of the first insulator film and an inner surface of a groove formed in the first insulator film by removing each dummy gate, to the extent that the groove is not completely buried;

a step of etching back the silicon nitride

film or the polysilicon film to form side walls on an inner surface of each groove; and

a step of implanting impurities of the first conductivity type to form a heavily impurity doped region having an impurity concentration higher than the first conductivity type region in the surface layer of the semiconductor substrate between the pair of source/drain diffusion lagers, by using the first insulator film and the side walls as a mask.

33. A manufacture method for a nonvolatile semiconductor memory device according to claim 32, wherein said step of implanting impurities implants impurities so that an impurity concentration of the first conductivity type regions between the source/drain diffusion layers and the heavily impurity doped region is lower than the impurity concentration of the heavily impurity doped region.

34. A manufacture method for a nonvolatile semiconductor memory device according to claim 32, further comprising:

a step of removing the side walls;

a step of forming a floating gate in each groove at least on a bottom and an inner surface thereof; and

a step of forming a control gate on a surface of the floating gate via a second insulator film.

35. A manufacture method for a nonvolatile semiconductor memory device, comprising:

a step of forming dummy gates on a semiconductor substrate having a first conductive type region on a surface thereof;

a step of forming a pair of source/drain diffusion layers of a second conductivity type in a surface layer of the semiconductor substrate between adjacent dummy gates, by using the dummy gates as a mask;

a step of burying the dummy gates with a first insulator film;

a step of removing a portion of the first insulator film to expose an upper surface of each dummy gates without exposing the surface of the semiconductor substrate;

a step of removing the dummy gates;

a step of depositing a silicon nitride film or a polysilicon film on an upper surface of the first insulator film and an inner surface of a groove formed in the first insulator film by removing each dummy gate, to the extent that the groove is not completely buried; and

a step of implanting impurities of the first conductivity type at an energy just allowing the impurities to transmit through the silicon nitride film or the polysilicon film deposited on a bottom of the groove, by using the first insulator film and the silicon nitride film or the polysilicon film on the first insulator film and on the inner surface of the

groove as a mask so as to form a heavily impurity doped region having an impurity concentration higher than the first conductivity type region in the surface layer of the semiconductor substrate between the pair of source/drain diffusion lagers.

36. A manufacture method for a nonvolatile semiconductor memory device according to claim 35, wherein said step of implanting impurities implants impurities so that an impurity concentration of the first conductivity type regions between the source/drain diffusion layers and the heavily impurity doped region is lower than the impurity concentration of the heavily impurity doped region.

37. A manufacture method for a nonvolatile semiconductor memory device according to claim 35, further comprising:

a step of removing the silicon nitride film or the polysilicon film;

a step of forming a floating gate in each groove at least on a bottom and an inner surface thereof; and

a step of forming a control gate on a surface of the floating gate via a second insulator film.

38. A manufacture method for a nonvolatile semiconductor memory device, comprising:

a step of forming dummy gates on a semiconductor substrate having a first conductive type region on a surface thereof;

a step of forming a pair of source/drain diffusion layers of a second conductivity type in a surface layer of the semiconductor substrate between adjacent dummy gates, by using the dummy gates as a mask;

a step of burying the dummy gates with a first insulator film;

a step of removing a portion of the first insulator film to expose an upper surface of each dummy gates without exposing the surface of the semiconductor substrate;

a step of removing the dummy gates;

a step of depositing a polysilicon film on an upper surface of the first insulator film and an inner surface of a groove formed in the first insulator film by removing each dummy gate, to the extent that the groove is not completely buried; and

a step of implanting impurities of the first conductivity type at an energy just allowing the impurities to transmit through the polysilicon film deposited on a bottom of the groove, by using at least the first insulator film and the polysilicon film on the inner surface of the groove as a mask so as to form a heavily impurity doped region having an impurity concentration higher than the first conductivity type region in the surface layer of the semiconductor substrate between the pair of source/drain diffusion lagers.

39. A manufacture method for a nonvolatile semiconductor memory device according to claim 38, wherein said step of implanting impurities implants impurities so that an impurity concentration of the first conductivity type regions between the source/drain diffusion layers and the heavily impurity doped region is lower than the impurity concentration of the heavily impurity doped region.

40. A manufacture method for a nonvolatile semiconductor memory device according to claim 38, further comprising:

a step of removing at least a portion of the polysilicon film on the first insulator film to form a floating gate; and

a step of forming a control gate on a surface of the floating gate via a second insulator film.

41. A manufacture method for a nonvolatile semiconductor memory device comprising:

a step of forming a well of a first conductivity type in a semiconductor substrate;

a step of forming a pair of semiconductor regions of a second conductivity type formed in the well of the first conductivity type, the pair of semiconductor regions being used as a source and a drain;

a step of forming a first gate on the semiconductor substrate via a first gate insulator; and

a step of forming a second gate on a second

insulator film covering the first gate,

wherein an impurity doped region of the first conductivity type having an impurity concentration higher than the well is formed in a channel region between the pair of semiconductor regions, the impurity doped region being not in contact with the semiconductor regions.

42. A manufacture method for a nonvolatile semiconductor memory device according to claim 41, wherein the semiconductor regions and the impurity region are formed in a self-alignment manner by tilted ion implantation tilted in opposite directions from a normal of the semiconductor substrate, by using the first gate as a mask.

43. A manufacture method for a nonvolatile semiconductor memory device according to claim 41, wherein the gate used as a mask for forming the impurity region through tilted ion implantation is one of a single layer film of polysilicon, a stacked film of a polysilicon film and a silicon oxide film, a stacked film of a polysilicon film and a silicon nitride film, and a stacked film of a polysilicon film, a silicon oxide film and a silicon nitride film.

44. A manufacture method for a nonvolatile semiconductor memory device according to claim 29, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

45. A manufacture method for a nonvolatile

semiconductor memory device according to claim 29, wherein the first conductivity type is an n-type and the second conductivity type is a p-type.

46. A manufacture method for a nonvolatile semiconductor memory device according to claim 44, wherein p-type impurities are boron or boron fluoride ions and n-type impurities are arsenic ions.

47. A manufacture method for a nonvolatile semiconductor memory device according to claim 45, wherein n-type impurities are phosphorous ions and p-type impurities are boron or boron fluoride ions.